2.(Amended) The display of claim 17, wherein a direction of array of said pixel TFTs is parallel or vertical to said side edge of said first substrate to which said nonconductive or weakly conductive material is applied or adhesively bonded.

6.(Amended) The display of claim 17, wherein said control circuit is packed over said first substrate by COG (chip-on-glass) technology.

10.(Amended) The method of claim 24, wherein said cutting step is carried out in such a way that a direction of array of said pixel TFTs is parallel or vertical to said cut side edges to which said nonconductive or weakly conductive material is applied or adhesively bonded.

14.(Amended) The method of claim 24, wherein said control circuit is packed over said first substrate by COG (chip-on-glass) technology.

17.(Amended) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

driver TFTs formed over said first substrate and forming a driver circuit for driving said pixel TFTs;

a bus line provided over said first substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said first substrate;

a nonconductive or weakly conductive material applied or adhesively bonded to a side edge of said counter substrate and a side edge of said first substrate;

a sealing material provided between said first substrate and said counter substrate and inside said side edge of said counter substrate and said side edge of said first substrate; and

a control circuit comprising a semiconductor chip provided under and in contact with said sealing material for controlling said driver circuit, said control circuit provided over said first substrate.

21. (Amended) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

driver TFTs formed over said first substrate and forming a driver circuit for driving said pixel TFTs;

a bus line provided over said first substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said first substrate;

a nonconductive or weakly conductive material applied or adhesively bonded to a side edge of said counter substrate and a side edge of said first substrate;

a sealing material provided between said first substrate and said counter substrate and inside said side edge of said counter substrate and said side edge of said first substrate; and

a control circuit comprising a semiconductor chip provided under and in contact with said sealing material for controlling said driver circuit, said control circuit provided over said first substrate.

22.(Amended) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

driver TFTs formed over said first substrate and forming a driver circuit for driving said pixel TFTs;

a bus line provided over said first substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said first substrate;

a nonconductive or weakly conductive material applied or adhesively bonded to a side edge of said counter substrate and a side edge of said first substrate;

a sealing material provided between said first substrate and said counter substrate and inside said side edge of said counter substrate and said side edge of said first substrate, said sealing material being provided outside at least said pixel TFTs; and

a control circuit comprising a semiconductor chip provided under and in contact with said sealing material for controlling said driver circuit, said control circuit provided over said first substrate.

23.(Amended) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

driver TFTs formed over said first substrate and forming a driver circuit for driving said pixel TFTs;

a bus line provided over said first substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said first substrate;

a nonconductive or weakly conductive material applied or adhesively bonded to a side edge of said counter substrate and a side edge of said first substrate;

a sealing material provided between said first substrate and said counter substrate and inside said side edge of said counter substrate and said side edge of said first substrate, said sealing material being provided outside said pixel TFTs and said driver TFTs; and

a control circuit comprising a semiconductor chip provided under and in contact with said sealing material for controlling said driver circuit, said control circuit provided over said first substrate.

24.(Amended) A method of fabricating an active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

driver TFTs formed over said first substrate and forming a driver circuit for driving said pixel TFTs;

a bus line provided over said first substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said first substrate;

a sealing material provided between said first substrate and said counter substrate and outside at least said pixel TFTs; and

a control circuit comprising a semiconductor chip provided under and in contact with said sealing material for controlling said driver circuit, said control circuit provided over said first substrate,

said method comprising:

cutting said first substrate and said counter substrate at a cut side edge of said first substrate and at a cut side edge of said counter substrate outside said sealing material having said control circuit under and in contact with said sealing material; and

applying or adhesively bonding a nonconductive or weakly conductive material to the cut side edge of said first substrate and the cut side edge of said counter substrate.

25. (Amended) A method of fabricating an active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a first substrate and arrayed in a matrix;

driver TFTs formed over said first substrate and forming a driver circuit for driving said pixel TFTs;

a bus line provided over said first substrate and connected with at least one of said pixel TFTs;

a counter substrate located opposite to said first substrate;

a sealing material provided between said first substrate and said counter substrate and outside said pixel TFTs and said driver TFTs; and

a control circuit comprising a semiconductor chip provided under and in contact with said sealing material for controlling said driver circuit, said control circuit provided over said first substrate,

said method comprising:

cutting said first substrate and said counter substrate at a cut side edge of said first substrate and at a cut side edge of said counter substrate outside said sealing material having said control circuit under and in contact with said sealing material; and

applying or adhesively bonding a nonconductive or weakly conductive material to the cut side edge of said first substrate and the cut side edge of said counter substrate.

27. (Amended) The display of claim 21, wherein a direction of array of said pixel TFTs is parallel or vertical to said side edge of said first substrate to which said nonconductive or weakly conductive material is applied or adhesively bonded.

31. (Amended) The display of claim 21, wherein said control circuit is packed over said first substrate by COG (chip-on-glass) technology.

32. (Amended) The display of claim 22, wherein a direction of array of said pixel TFTs is parallel or vertical to said side edge of said first substrate to which said nonconductive or weakly conductive material is applied or adhesively bonded.

36. (Amended) The display of claim 22, wherein said control circuit is packed over said first substrate by COG (chip-on-glass) technology.

37. (Amended) The display of claim 23, wherein a direction of array of said pixel TFTs is parallel or vertical to said side edge of said first substrate to which said nonconductive or weakly conductive material is applied or adhesively bonded.

41. (Amended) The display of claim 23, wherein said control circuit is packed over said first substrate by COG (chip-on-glass) technology.

51. (Amended) The display of claim 17, wherein said sealing material is apart from said side edge of said counter substrate and said side edge of said first substrate.

52. (Amended) The display of claim 21, wherein said sealing material is apart from said side edge of said counter substrate and said side edge of said first substrate.

53. (Amended) The display of claim 22, wherein said sealing material is apart from said side edge of said counter substrate and said side edge of said first substrate.

54. (Amended) The display of claim 23, wherein said sealing material is apart from said side edge of said counter substrate and said side edge of said first substrate.

55. (Amended) The method of claim 24, wherein said sealing material is apart from said side edge of said counter substrate and said side edge of said first substrate.

56. (Amended) The method of claim 25, wherein said sealing material is apart from said side edge of said counter substrate and said side edge of said first substrate.

61. (Amended) A semiconductor device comprising:

a pixel TFT provided over a first substrate comprising a glass;

a channel formation region provided in a semiconductor film provided over said first substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween;

a counter substrate located opposite to said first substrate;

a bus line provided over said first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said first substrate;

a sealing material provided between said first substrate and said counter substrate; and

a nonconductive material applied to a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line,

wherein said nonconductive material is provided on an outer side of said sealing material, and

wherein said gate insulating film has a thickness of 500 to 2000 Å.

62.(Amended) A semiconductor device comprising:

a pixel TFT provided over a first substrate comprising a glass;

a channel formation region provided in a semiconductor film provided over said first substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween;

a counter substrate located opposite to said first substrate;

a bus line provided over said first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said first substrate;

a sealing material provided between said first substrate and said counter substrate; and

a weakly conductive material applied to a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line,

wherein said weakly conductive material is provided on an outer side of said sealing material, and

wherein said gate insulating film has a thickness of 500 to 2000 Å.

63. (Amended) A semiconductor device comprising:

a pixel TFT provided over a first substrate comprising a glass;

a channel formation region provided in a semiconductor film provided over said first substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween;

a driver TFT provided over said first substrate;

a counter substrate located opposite to said first substrate;

a bus line provided over said first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said first substrate;

a sealing material provided between said first substrate and said counter substrate; and

a nonconductive material applied to a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line,

wherein said nonconductive material is provided on an outer side of said sealing material, and

wherein said gate insulating film has a thickness of 500 to 2000 Å.

64. (Amended) A semiconductor device comprising:

a pixel TFT provided over a first substrate comprising a glass;

a channel formation region provided in a semiconductor film provided over said first substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween;

a driver TFT provided over said first substrate;

a counter substrate located opposite to said first substrate;

a bus line provided over said first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said first substrate;

a sealing material provided between said first substrate and said counter substrate; and

a weakly conductive material applied to a side edge of said counter substrate and said side edge of said first substrate and said part of said bus line,

wherein said weakly conductive material is provided on an outer side of said sealing material, and

wherein said gate insulating film has a thickness of 500 to 2000 Å.

65. (Amended) The display of claim 17 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said first substrate.

66. (Amended) The display of claim 21 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said first substrate.

67. (Amended) The display of claim 22 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said first substrate.

68. (Amended) The display of claim 23 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said first substrate.

69. (Amended) The display of claim 61 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said first substrate.

70. (Amended) The display of claim 62 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said first substrate.

71. (Amended) The display of claim 63 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said first substrate.

72. (Amended) The display of claim 64 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said first substrate.